Opto-Compatible Single Channel Isolated Gate Driver

GENERAL DESCRIPTION

The SiLM5384 isolated driver family is an opto-compatible, single channel, isolated MOSFET, IGBT gate driver with different UVLO voltage level. The peak output current is 4.0A. Key features and characteristics bring significant performance and reliability upgrades over standard opto-coupler based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high common mode transient immunity (CMTI), low propagation delay, and small pulse width distortion.

The input stage is an emulated diode which means long term reliability and excellent aging characteristics compared to traditional LEDs. It is offered in a SOP6W-T and SMP8 package. A mold compound from material group I which has a comparative tracking index (CTI) >600V. High performance and reliability of the SiLM5384 makes it ideal for use in all types of motor drives, solar inverters, industrial power supplies, and appliances.

APPLICATION

- AC and brushless DC motor drives
- Renewable energy inverters
- Industrial power supplies

FEATURES

- Driver output current: 4A
- 110ns (Max.) propagation delay
- 35ns (Max.) pulse width distortion
- 200kV/us common mode transient immunity (CMTI)
- Wide gate drive supply voltage
  - 10 V to 30 V for SiLM5384B
  - 14 V to 30 V for SiLM5384D
- 7V reverse polarity voltage handling capability on input stage
- Pin to pin compatible to opto-coupler isolated gate drivers
- Package: SOP6W-T and SMP8
- Junction temperature, T_J: -40°C to +150°C
- Safety certifications
  - 5.7kV$_{RMS}$ isolation for 1 minute per UL 1577 for SOP6W-T
  - 5kV$_{RMS}$ isolation for 1 minute per UL 1577 for SMP8
  - CQC certification per GB4943.1-2022
  - DIN VDE 0884-17: 2021-10

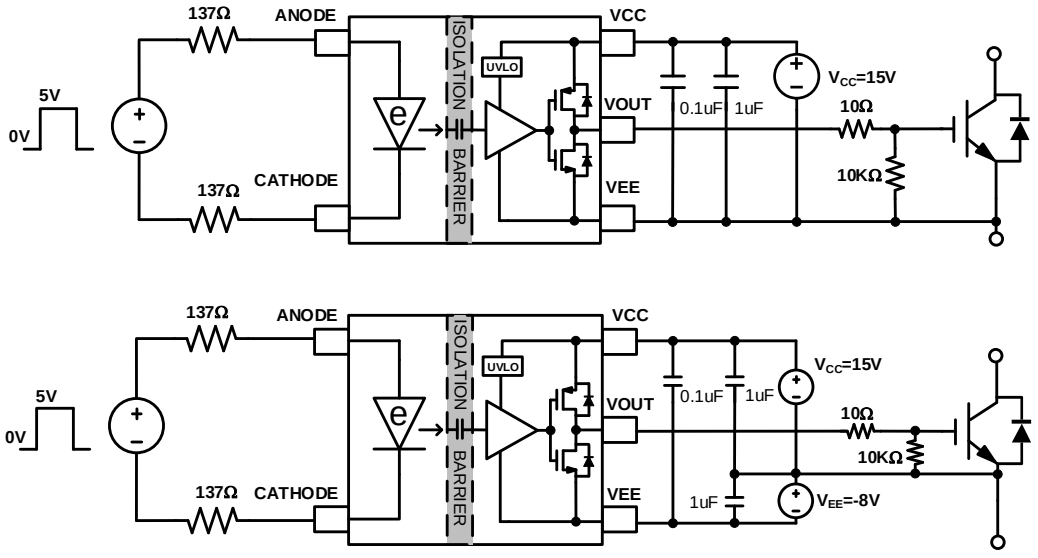
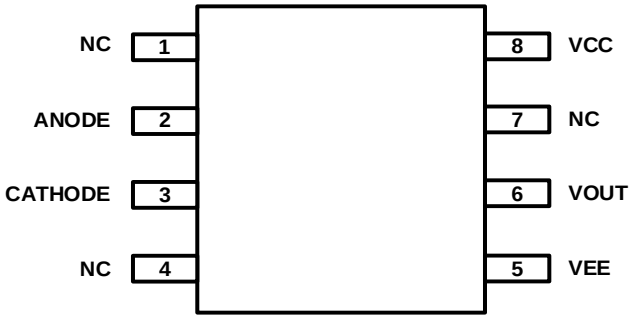


Figure 1. SiLM5384 Single and Bipolar Power Supplies Application Circuit to Drive IGBT

Table of Contents

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP6W-T	
SMP8	

PIN DESCRIPTION

Pin Name	PIN No.		Description
	SOP6W-T	SMP8	
ANODE	1	2	Anode
CATHODE	3	3	Cathode
VEE	4	5	Negative Power Supply Rail
VOUT	5	6	Gate Drive Output
VCC	6	8	Positive Power Supply Rail
NC	2	1, 4, 7	No Connection

FUNCTIONAL BLOCK DIAGRAM

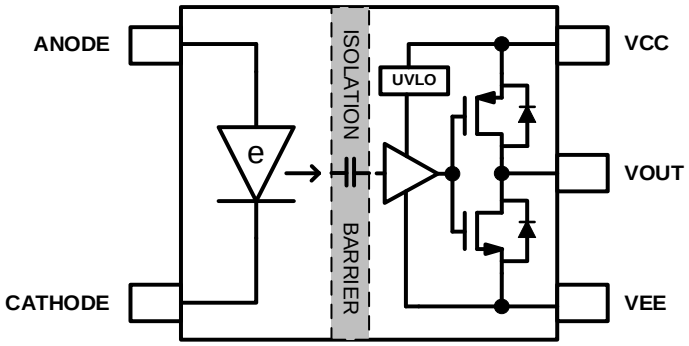


Figure 2. SiLM5384 Functional Block Diagram

ORDERING INFORMATION

Order Part No.	Output Current	UVLO	Package	QTY
SiLM5384DCR-DG	4A	12.5V	SOP6W-T, Pb-Free	1000/Reel
SiLM5384BCR-DG	4A	8.5V	SOP6W-T, Pb-Free	1000/Reel
SiLM5384DDC-DG	4A	12.5V	SMP8, Pb-Free	800/Reel
SiLM5384BDC-DG	4A	8.5V	SMP8, Pb-Free	800/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
$I_{F(AVG)}$	Average input current		25	mA
$I_{F(TRAN)}$	Peak transient input current, t_{PULSE}<1us		0.7	A
V_R	Reverse Input Voltage		7	V
V_{CC} -V_{EE}	Output supply voltage	-0.3	35	V
V_{OUT}	Driver output votlage	V_{EE}-0.3	V_{CC}+0.3	V
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

RECOMMENDED OPERTION CONDITIONS

Symbol	Definition	Min	Max	Unit
V_{CC} -V_{EE}	Output Supply Voltage (12.5V UVLO)	14	30	V
	Output Supply Voltage (8.5V UVLO)	10	30	V
I_F(ON)	Input Diode Forward Current (Diode “ON”)	7	16	mA
V_F(OFF)	Anode Voltage - Cathode Voltage (Diode “OFF”)	-5.5	0.9	V
T_J	Junction temperature	-40	150	°C
T_A	Ambient temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Unit
V_{ESD}	HBM	±3000	V
	CDM	±2000	

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP6W-T	SMP8	
$R_{\theta JA}$	Junction to ambient thermal resistance	125	66	°C/W
$R_{\theta JC}$	Junction to case (top) thermal resistance	66	36	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min	Typ	Max	Units
R_{IO}	Resistance (Input Side to Output Side)		10^{12}		Ω
C_{IO}	Capacitance (Input Side to Output Side)		0.8		pF
C_{IN}	Input Capacitance		30		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP6W-T	SMP8	
CLR	External clearance	Shortest terminal to terminal distance through air	≥8	⩾7	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	≥8	⩾7	mm
DTI	Distance through the insulation	Minimum internal gap	24	24	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I	I	
	Overvoltage category	Rated mains voltages ≤150Vrms	IV	IV	
		Rated mains voltages ≤300Vrms	IV	IV	
		Rated mains voltages ≤600Vrms	IV	III	
		Rated mains voltages ≤1000Vrms	III	II	
DIN V VDE 0884-11					
V_{IORM}	Maximum repetitive peak isolation voltage		2121	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (Sine wave)	1500	1060	V_{RMS}
		DC voltage	2121	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	60s	8000	7000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC62368, 1.2/50us waveform, V_{TEST}=1.6 x V_{IOSM}	6250	6250	V_{PK}
q_{pd}	Apparent charge	Method b2: $V_{pd(m)}$=1.875 x V_{IORM}, tm=1 s	≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
UL1577					
V_{ISO}	Withstand Isolation Voltage	V_{TEST}=V_{ISO}, t=60s (qualification), V_{TEST}=1.2 x V_{ISO}, t=1s (100% production)	5700	5000	V_{RMS}

SAFETY RELATED CERTIFICATIONS FOR SOP6W-T

VDE	UL	CQC	TUV
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to EN IEC 61010-1: 2010+A1 and EN IEC 62368-1: 2018
Reinforced Insulation	Single protection, 5700V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate	Reinforced insulation, 1500Vrms working voltage
Pending	Certificate Number: UL-US-2128883-9	File Number: CQC23001379623	Ref.Certif.No: DE 2-047148 Ref.Certif.No: JPTUV-189379 Certificate No: R 50735450 0001

SAFETY LIMITING VALUES FOR SOP6W-T

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=125°C/W, V_{CC}-V_{EE} = 15V, T_J =150°C, T_A =25°C	50	mA
		$R_{\theta JA}$=125°C/W, V_{CC}-V_{EE} = 30V, T_J =150°C, T_A =25°C	25	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=125°C/W, T_J =150°C, T_A =25°C	750	mW
T_S	Maximum safety temperature		150	°C

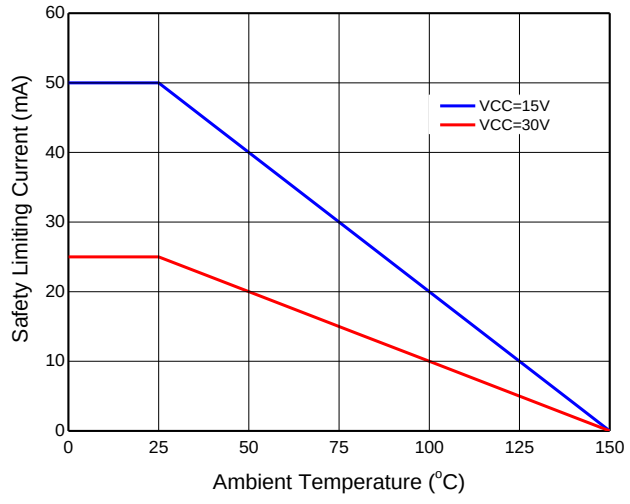


Figure 3. Thermal Derating Curve for Limiting Current per VDE for SOP6W-T

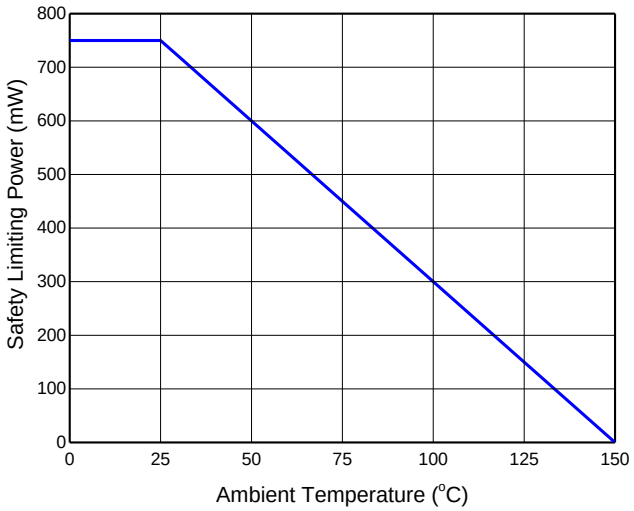


Figure 4. Thermal Derating Curve for Limiting Power per VDE for SOP6W-T

SAFETY RELATED CERTIFICATIONS FOR SMP8

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Reinforced Insulation	Single protection, 5000V_{RMS}	Reinforced insulation, Altitude≤ 5000m, Tropical climate
Pending	Pending	Pending

SAFETY LIMITING VALUES FOR SMP8

Symbol	Parameter	Condition	Value	Unit
I_S	Safety input, output, or supply current	$R_{\theta JA}$=66°C/W, V_{CC}-V_{EE} = 15V, T_J =150°C, T_A =25°C	80	mA
		$R_{\theta JA}$=66°C/W, V_{CC}-V_{EE} = 30V, T_J =150°C, T_A =25°C	40	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$=66°C/W, T_J =150°C, T_A =25°C	1200	mW
T_S	Maximum safety temperature		150	°C

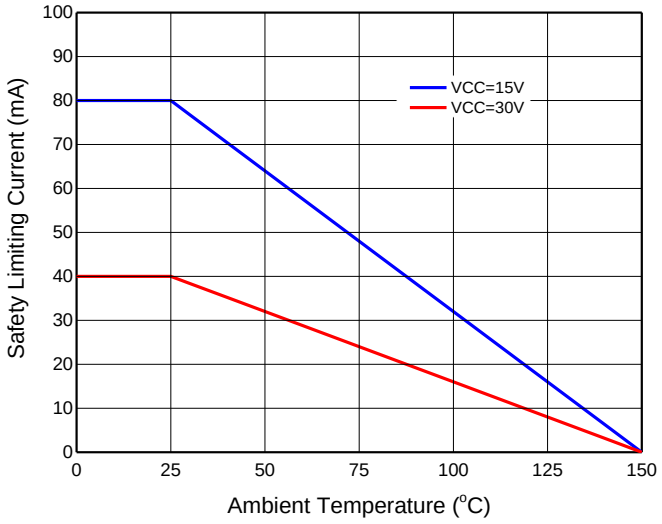


Figure 5. Thermal Derating Curve for Limiting Current per VDE for SMP8

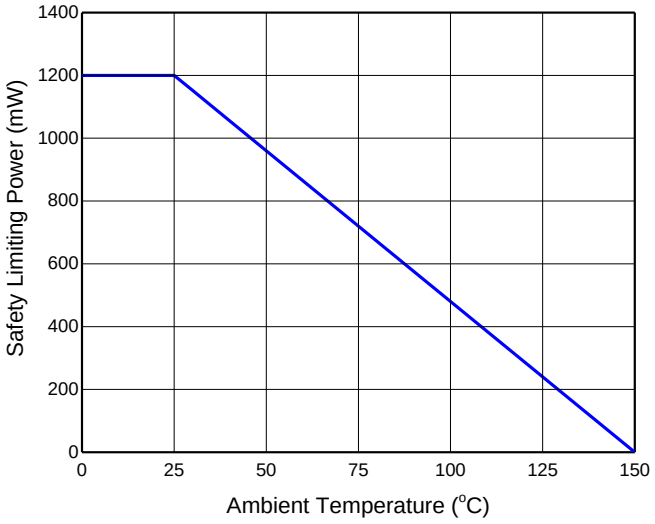


Figure 6. Thermal Derating Curve for Limiting Power per VDE for SMP8

ELECTRIAL CHARACTERISTICS (DC)

V_{CC}-V_{EE} = 15V, V_{EE} = GND at T_A = 25°C unless otherwise specified. All min and max specifications are at T_A= -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
INPUT						
I_{FLH}	Input Forward Threshold Current Low to High	V_{OUT}>5V, C_{LOAD}=1nF		1.7	3	mA
V_F	Input Forward Voltage	I_F=10mA	2.0	2.2	2.5	V
V_{F_HL}	Input Threshold Voltage, High to Low	V_{OUT}<5V, C_{LOAD}=1nF	0.9			V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	I_F=10mA		1		mV/°C
V_R	Input Reverse Breakdown Voltage	I_R=10uA	7			V
OUTPUT						
I_{OH}	High Level Peak Output Current	V_{CC}=15V, I_F=10mA, C_{VCC}=10uF, C_{LOAD}=220nF		4.0		A
I_{OL}	Low Level Peak Output Current	V_{CC}=15V, V_F=0V, C_{VCC}=10uF, C_{LOAD}=220nF		6.0		A
V_{OH}	High Level Output Voltage	I_F=10mA, I_O= -20mA “With respect to Vcc”		23		mV
V_{OL}	Low Level Output Voltage	V_F=0V, I_O=20mA		10		mV
UNDER VOLTAGE LOCKOUT(SiLM5384D)						
$UVLO_R$	Under Voltage Lockout V_{CC} rising	I_F=10mA	11.5	12.5	13.5	V
$UVLO_F$	Under Voltage Lockout V_{CC} falling	I_F=10mA	10.5	11.5	12.5	V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			1.0		V
UNDER VOLTAGE LOCKOUT (SiLM5384B)						
$UVLO_R$	Under Voltage Lockout V_{CC} rising	I_F=10mA	8	8.5	9	V
$UVLO_F$	Under Voltage Lockout V_{CC} falling	I_F=10mA	7	7.5	8	V
$UVLO_{HYS}$	Under Voltage Lockout Hysteresis			1.0		V
DRIVER SUPPLY CURRENT						
I_{CCH}	VCC Quiescent Current When Output High	I_F=10mA, I_O=0mA		2.3	3.3	mA
I_{CCL}	VCC Quiescent Current When Output Low	V_F=0V, I_O=0mA		1.5	2.4	mA

SWITCHING CHARACTERISTICS (AC)

V_{CC}-V_{EE} = 15V, V_{EE} = GND at T_A = 25°C unless otherwise specified. All min and max specifications are at T_A= -40°C to 125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{PLH}	Propagation delay, Low to High	C_{LOAD} =1nF, I_F=10mA, f_{sw}=20kHz, (50% Duty Cycle), V_{CC}=15V		60	110	ns
t_{PHL}	Propagation delay, High to Low			60	110	ns
t_{PWD}	Pulse Width Distortion				35	ns
t_{PDD}	Propagation Delay Difference Between Any Two Parts		-25		25	ns
t_r	Turn on rise time	C_{LOAD} =1nF			25	ns
t_f	Turn off fall time	C_{LOAD} =1nF			20	ns
t_{UVLO_REC}	UVLO Recovery Delay	V_{CC} Rising from 0V to 15V		10	30	us
$CMTI_H$	Output High Level Common Mode Transient Immunity	I_F=10mA, V_{CM}=1000V, V_{CC}=15V, T_A=25°C	150	200		kV/us
$CMTI_L$	Output Low Level Common Mode Transient Immunity	V_F=0V, V_{CM}=1000V, V_{CC}=15V, T_A=25°C	150	200		kV/us

PARAMETER MEASUREMENT INFORMATION

Propagation Delay, Rise Time and Fall Time

Figure 7 shows the propagation delay from the input forward current I_F to V_{OUT}. This figure also shows the circuit used to measure the rise (t_r)and fall(t_f) times and the propagation delays t_{PLH} and t_{PHL}.

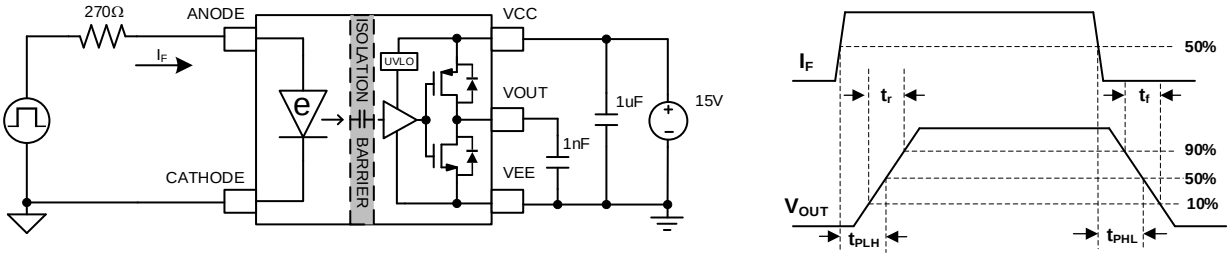


Figure 7. Propagation Delay, Rise Time and Fall Time

IOH and IOL Testing

Figure 8 shows the circuit used to measure the output drive current I_{OL} and I_{OH}. A load capacitance of 220nF is used at the output. The peak dv/dt of the capacitor voltage is measured in order to determine the peak source and sink currents of the gate driver.

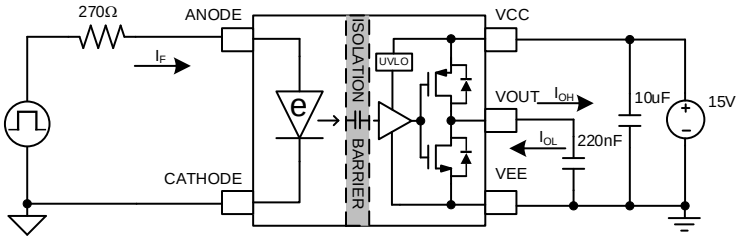


Figure 8. I_{OH} and I_{OL}

CMTI Testing

Figure 9 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V. The test is performed with I_F=10mA (V_{OUT}= High) and V_F=0V (V_{OUT}= Low).

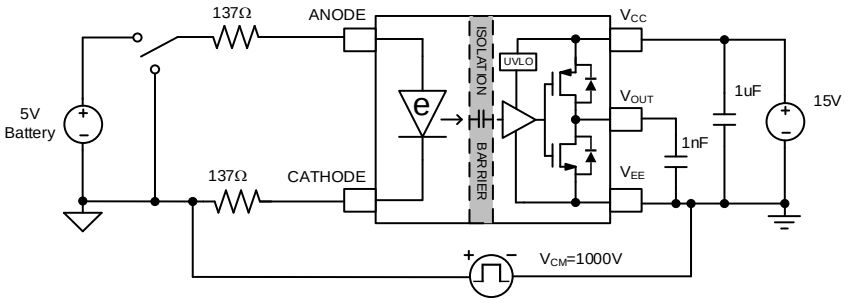


Figure 9. CMTI Test Circuit

FEATURE DESCRIPTION

SiLM5384 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs and MOSFETs. It has 4.0A peak output current capability with maxim output driver supply voltage of 30V. The inputs and the outputs are galvanically isolated. SiLM5384 is offered in SOP6W-T and SMP8. The reinforced isolation rating is 5700V_{RMS} in SOP6W-T and 5000V_{RMS} in SMP8 for 60 seconds. It is pin-to-pin compatible with standard opto-coupler isolated gate drivers. While standard opto-coupler isolated gate drivers use an LED as the input stage, SiLM5384 uses an emulated diode as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by dual, series HV SiO2 capacitors in full differential configuration that not only provides reinforced isolation but also offers great performance of common mode transient immunity >150kV/us. The e-diode input stage along with capacitive isolation technology gives SiLM5384 several performance advantages over standard opto-coupler isolated gate drivers.

- Since the emulated diode does not use light emission for its operation, the reliability and aging characteristics of SiLM5384 are naturally superior to those of standard opto-coupler isolated gate drivers.
- Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto-coupler isolated gate drivers
- The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature
- Higher common mode transient immunity than opto-coupler isolated gate drivers
- Smaller propagation delay than opto-coupler isolated gate drivers
- Due to superior process controls achievable in capacitive isolation compared to opto-coupler isolation, there is less part-to-part skew in the propagation delay, making the system design simpler and more robust
- Smaller pulse width distortion than opto-coupler isolated gate drivers

Input Stage

The input stage of SiLM5384 is an emulated diode. When the emulated diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current, I_F, flows into the e-diode. The forward voltage drop across the e-diode is 2.2V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 7mA to 16mA. When I_F exceeds the input forward threshold current I_{FLH} , the V_{OUT} is driver high. If the I_F is lower than I_{FLH}, or the voltage between Anode and Cathode is reverse biased, the V_{OUT} is driven low.

The reverse breakdown voltage of the e-diode is up to 7V. The large reverse breakdown voltage of the e-diode enables SiLM5384 to be operated in interlock architecture as shown in Figure 10. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown in Figure 10 and driven by two buffers that are controlled by the MCU. Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs as shown in Figure 11. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

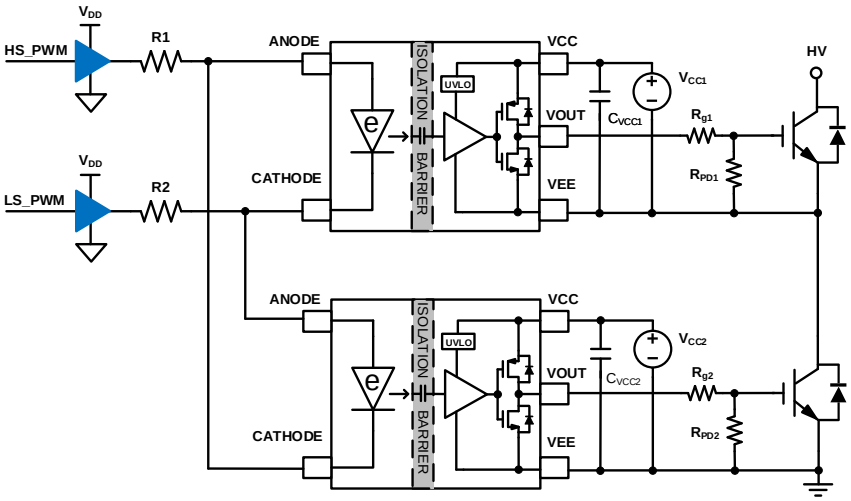
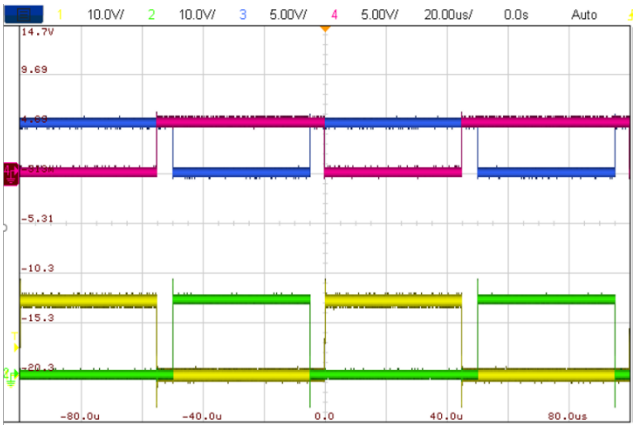


Figure 10. Interlock Architecture



CH1: HS_OUT, CH2: LS_OUT, CH3: HS_PWM, CH4: LS_PWM

Figure 11. Interlock PWM input and output waveform

Under Voltage Lockout (UVLO)

The SiLM5384 integrates the UVLO protection on the V_{CC} to prevent an under driven condition on IGBTs and MOSFETs. When V_{CC} is lower than $UVLO_R$ during start up or lower than $UVLO_F$ after start up, the UVLO feature holds the V_{OUT} low, regardless of the input forward current. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply. When V_{CC} drops below $UVLO_F$, a recovery delay (t_{UVLO_REC}) occurs on the output when the supply voltage rises above $UVLO_R$ again.

Device Functional Mode

Table 1 shows the functional modes for SiLM5384.

Table 1. Driver functional table

E-Diode	VCC Status	Output
X	Powered Down	Low
$I_F>I_{FLH}$	Powered Up	High
$V_F<V_{F\_HL}$	Powered Up	Low

X: Irrelevant; Powered Up: V_{CC} > UVLO threshold; Powered Down: V_{CC} < UVLO threshold;

Typical Input Configuration Circuit

The circuit in Figure 12 and Figure 13 show two typical input configuration circuits for SiLM5384 to driver IGBT.

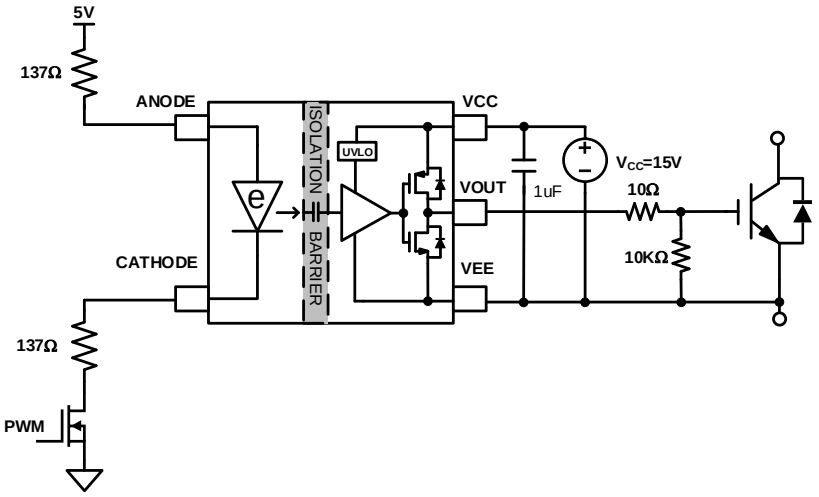


Figure 12. Single MOSFET Circuit as Input Drive of SiLM5384 to Drive IGBT

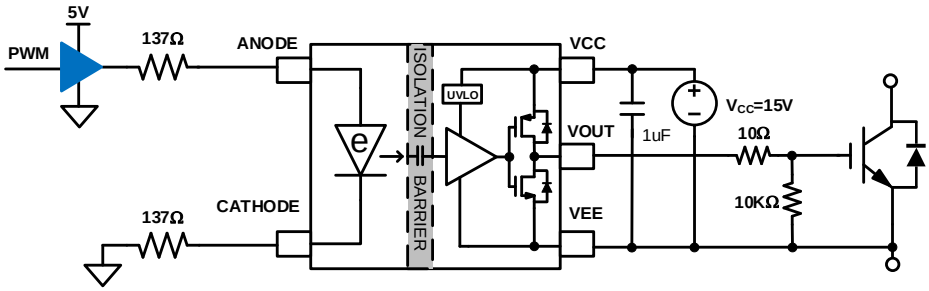


Figure 13. Buffer Circuit as Input Drive of SiLM5384 to Drive IGBT

Layout

In order to achieve optimum performance for the SiLM5384, some suggestions on PCB layout.

Component placement:

- Low ESR and low ESL capacitors must be connected close to the device between the VCC and VEE pins to bypass noise and to support high peak currents when turning on the external power transistor.
- To avoid large negative transients on the VEE pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.

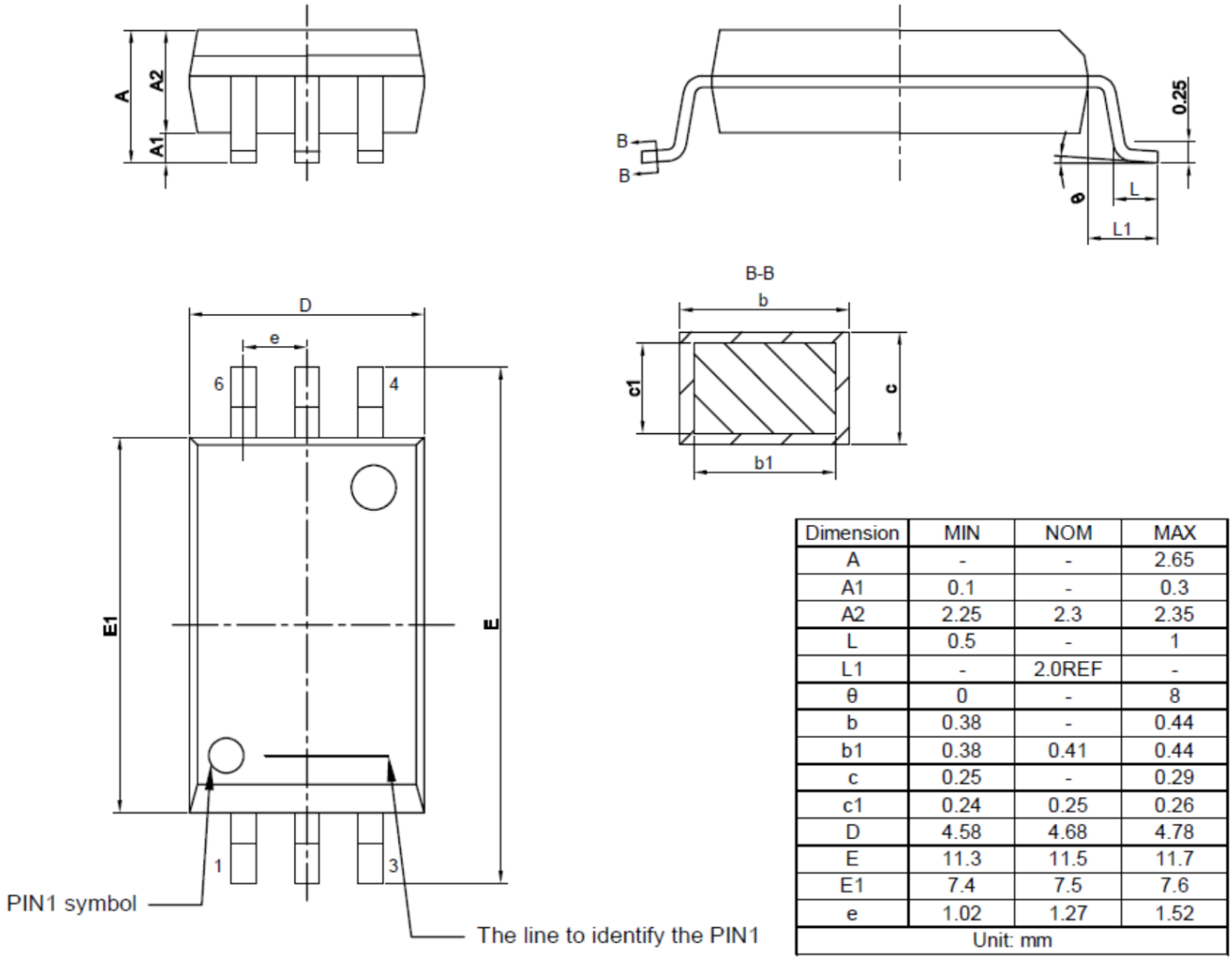
Grounding considerations:

- Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.

High-voltage considerations:

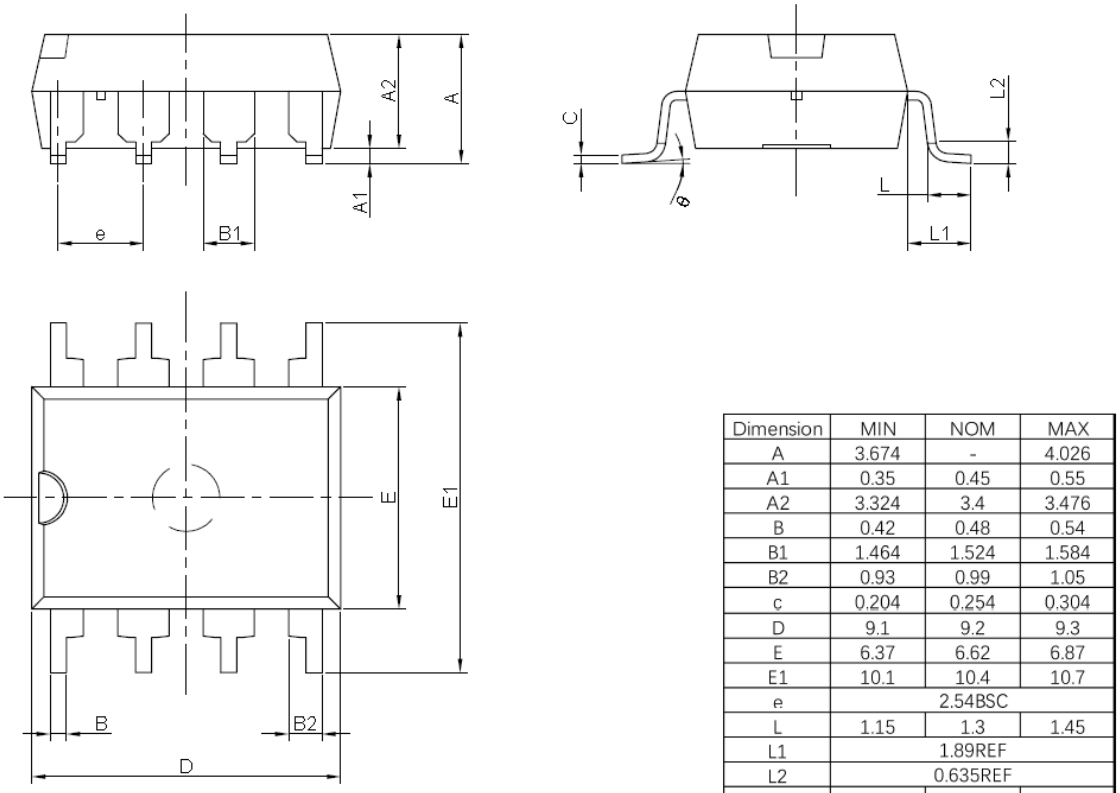
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	2.65
A1	0.1	-	0.3
A2	2.25	2.3	2.35
L	0.5	-	1
L1	-	2.0REF	-
θ	0	-	8
b	0.38	-	0.44
b1	0.38	0.41	0.44
c	0.25	-	0.29
c1	0.24	0.25	0.26
D	4.58	4.68	4.78
E	11.3	11.5	11.7
E1	7.4	7.5	7.6
e	1.02	1.27	1.52
Unit: mm			

Figure 14. SOP6W-T Package Outline Dimensions



Dimension	MIN	NOM	MAX
A	3.674	-	4.026
A1	0.35	0.45	0.55
A2	3.324	3.4	3.476
B	0.42	0.48	0.54
B1	1.464	1.524	1.584
B2	0.93	0.99	1.05
c	0.204	0.254	0.304
D	9.1	9.2	9.3
E	6.37	6.62	6.87
E1	10.1	10.4	10.7
e	2.54BSC		
L	1.15	1.3	1.45
L1	1.89REF		
L2	0.635REF		
θ	0°	-	8°

Figure 15. SMP8 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: May/2026	
Whole document	Initial datasheet release.